

REMARKS

Reconsideration of this application is requested. Claims 2-15 and 17-24 are active in the application subsequent to entry of this Amendment.

The examiner's attention is directed to an Information Disclosure Statement filed September 30, 2002, subsequent to mailing of the Official Action, for which the relevant fee has been paid in order to secure consideration of the IDS. In due course consideration of the IDS is requested.

Responsive to items 1-3 in the Official Action, a new title for the invention has been provided as suggested by the examiner and the Abstract has been amended in order to agree with Figures 4-7 of the drawings. Applicants appreciate the examiner's care and attention in noting this. The specification is believed to be appropriate as minor errors have not been detected.

The claims have been amended in order to more particularly point out and distinctly claim that which applicants regard as their invention. More specifically, claims 1 and 16 have been combined and now appear as new claim 24 while the dependencies of various dependent claims have been adjusted accordingly.

The Official Action contains two prior art-based rejections (see items 4-7) and of these claim 16 is only involved in the first rejection (items 4-5). Accordingly, it will not be necessary to address the second rejection but attention will be focused on the rejection of alleged anticipation.

Original claims 1, 5, 6, 10 and 16 have been rejected as allegedly being anticipated by U.S. 6,252,894 to Sasanuma et al which is applied as of its actual U.S. filing date of March 5, 1999. (This patent issued subsequent to the priority dates claimed in the present application.)

Responding to the detailed comments provided in item 5 of the Official Action, the examiner argues that the layer 119 in Sasanuma corresponds to the first barrier layer of the present invention. This is not so – as discussed below, the layer 119 in Sasanuma

does not correspond to the "first barrier layer" but to the "electron confinement layer" of the present invention.

The "first barrier layer" in the present invention as defined in applicants' claims is a part of the active layer having a quantum well structure that consists of at least one well layer and a plurality of barrier layers. The "first barrier layer" is one "arranged in the nearest portion to said p-type nitride semiconductor layer among said barrier layers". Adjoining the active layer on the p-side is the "electron confinement layer" made of nitride semiconductor including Al.

The electron confinement layer serves as an electron barrier to confine electrons within active layer (see, section [0086]). The electron confinement layer also supplies p-type impurity, for example Mg, to the "first barrier layer" through diffusion (see, section [0087]). Since the "first barrier layer" does not substantially include the n-type impurity, the coexistence of the n-type impurity and p-type impurity is prevented, which improves the lifetime of the device (see, section [0011]).

The reference is concerned with a distinctly different structure. In Sasanuma, "the active layer has a multiple quantum well structure constructed by a periodic structure in which two types of InAlGaN layers having a thickness of 10mm or less are alternatively disposed" (column 5, lines 50-53). In other words, the active layer in Sasanuma consists of InAlGaN well layers and InAlGaN barrier layers.

Adjoining the active layer on p-side is the "p-type thin film barrier layer 119" "formed on Mg doped p-AlGaN" (column 5, lines 53-55). The thin film barrier layer 119 made of p-AlGaN, which will be apparent from its name, serves as an electron barrier to confine electrons within the active layers. The thin film layer 119 also supplies p-type impurity, i.e. Mg, to the InAlGaN barrier layers in the active layer by diffusion, because the thin film layer 119 is doped with Mg. Thus, the layer 119 in Sasanuma does **not** correspond to the "first barrier layer" but to the "electron confinement layer" of the present invention.

Accordingly, Sasanuma merely describes an ordinary multiple quantum well structure and discloses nothing about an impurity doping to the barrier layers of the

quantum well structure. Thus, claims 2-15 and 17-24 are not disclosed or suggested by Sasanuma.

From the above discussion it will be apparent that the Sasanuma et al reference does not satisfy the requisite to establish anticipation. To anticipate a claim, a single reference must disclose the claimed invention with sufficient clarity to prove its existence in the prior art. *Motorola Inc. v. Interdigital Technology Corp.*, 43 USPQ2d 1481, 1490 (Fed. Cir. 1997). Anticipation rejections are only proper when the "claimed subject matter is identically disclosed or described in 'the prior art', without *any* need for picking, choosing, and combining various disclosures not directly related to each other by the teachings of the cited reference." *In re Arkley*, 172 USPQ 524, 526 (CCPA 1972); *see also Akzo N.V. v. International Trade Commission*, 1 USPQ 2d 1241, 1246 (Fed. Cir. 1986); *Ex parte Lee*, 31 USPQ 2d 1105, 1108 (BPAI 1993). Every element of the challenged claim must be disclosed within this single reference. *PPG Industries Inc. v. Guardian Industries Corp.*, 37 USPQ2d 1618, 1624 (Fed. Cir. 1996). Absence from the reference of any claimed element negates anticipation *Kloster Speedsteel AB v. Crucible Inc.* 23 USPQ 160 (Fed. Cir. 1986).

Thus, applicants' claims are patentable over Sasunuma et al since it fails to disclose each element of applicants' claims.

Reconsideration and favorable action are solicited.

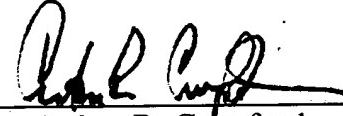
Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page(s) is captioned "Version With Markings To Show Changes Made."

KOZAKI

Serial No. 09/898,460

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

2. (Amended) The nitride semiconductor device according to Claim [1] 24, wherein the film thickness of said first barrier layer is greater than the film thickness of said second barrier layer.

3. (Amended) The nitride semiconductor device according to Claim [1] 24, wherein said active layer has L ($L \geq 2$) barrier layers so that the barrier layer arranged in a position nearest to said n-type nitride semiconductor layer is denoted as barrier layer B_1 and the i-th barrier layer ($i=1, 2, 3, \dots L$) counted from the barrier layer B_1 toward said p-type nitride semiconductor layer is denoted as barrier layer B_i ; and barrier layers B_i from $i=1$ to $i=n$ ($1 < n < L$) include an n-type impurity.

4. (Amended) The nitride semiconductor device according to Claim [1] 24, wherein the entire barrier layers other than said first barrier layer include an n-type impurity.

5. (Amended) The nitride semiconductor device according to Claim [1] 24, wherein said first barrier layer is arranged in the outermost position in said active layer.

6. (Amended) The nitride semiconductor device according to Claim [7] 24, wherein said second barrier layer is arranged in the outermost position close to said n-type nitride semiconductor layer within said active layer.

9. (Amended) The nitride semiconductor device according to Claim [1] 24, wherein at least one well layer within said active layer has a film thickness of not less than 40 Å.

10. (Amended) The nitride semiconductor device according to Claim [1] 24, wherein said first barrier layer has a p-type impurity.

11. (Amended) The nitride semiconductor device according to Claim [1] 24, wherein said first barrier layer includes a p-type impurity in the range of no less than $5 \times 10^{16} \text{ cm}^{-3}$ and no more than $1 \times 10^{19} \text{ cm}^{-3}$.

12. (Amended) The nitride semiconductor device according to Claim [1] 24, wherein said first barrier layer is p-type or i-type.

14. (Amended) The nitride semiconductor device according to Claim [1] 24, wherein said n-type nitride semiconductor layer, said active layer and said p-type nitride semiconductor layer are layered in sequence.

15. (Amended) The nitride semiconductor device according to Claim [1] 24, wherein said p-type nitride semiconductor layer has an upper clad layer made of a nitride semiconductor that includes Al of which the average mixed crystal ratio x is in the range of $0 < x \leq 0.05$;

said n-type nitride semiconductor layer has a lower clad layer made of a nitride semiconductor that includes Al of which the average mixed crystal ratio x is in the range of $0 < x \leq 0.05$; and

the nitride semiconductor device has a laser device structure.

21. (Amended) The nitride semiconductor device according to Claim 24, wherein said p-type nitride semiconductor layer has an upper clad layer made of a nitride semiconductor that includes Al and said n-type nitride semiconductor layer has a lower clad layer made of a nitride semiconductor, wherein the average mixed crystal ratio of Al in the upper clad layer is greater than that of the lower clad layer.

23. (Amended) The nitride semiconductor device according to Claim 24, wherein said active layer has a well layer of which distance dB from the first p-type nitride semiconductor layer is in the range of no less than 100 Å and no more than 400 Å and has a first barrier layer within the distance dB.

Add the following new claim:

--24. (new) A nitride semiconductor device wherein an active layer is sandwiched between p-type nitride semiconductor layers and n-type nitride semiconductor layers, wherein said p-type nitride semiconductor layers has an electrons confining layer adjoining said active layer and made of nitride semiconductor that includes Al; and said active layer has a quantum well structure including at least one well layer made of nitride semiconductor that includes In and barrier layers made of nitride semiconductor, wherein a first barrier layer arranged in the nearest position to said p-type nitride semiconductor layer among said barrier layers substantially does not have an n-type impurity, while a second barrier layer that is different from said first barrier layer has an n-type impurity.--

17. (Amended) The nitride semiconductor device according to Claim [16] 24, wherein said first p-type nitride semiconductor layer is provided so as to contact a barrier layer nearest to said p-type nitride semiconductor layer and has been grown being doped with a p-type impurity of which concentration is higher than that of said barrier layer in said active layer.

18. (Amended) The nitride semiconductor device according to Claim [1] 24, wherein the number of well layers in said active layer is from 1 to 3.

19. (Amended) The nitride semiconductor device according to claim [1] 24, in said active layer said second barrier layer is arranged between well layers and the film thickness ratio R_t (= [film thickness of a well layer] / [film thickness of a barrier layer]) of said well layer to the second barrier layer is in the range of $0.5 \leq R_t \leq 3$.

20. (Amended) The nitride semiconductor device according to claim [1] 24, wherein the film thickness d_w of said well layer is in the range of $40 \text{ \AA} \leq d_w \leq 100 \text{ \AA}$ while the film thickness d_b of said second barrier layer is in the range of $d_b \geq 40 \text{ \AA}$.

21. (Amended) The nitride semiconductor device according to Claim [1] 24, wherein said p-type nitride semiconductor layer has an upper clad layer made of a nitride semiconductor that includes Al and said n-type nitride semiconductor layer has a lower clad layer made of a nitride semiconductor, wherein the average mixed crystal ratio of Al in the upper clad layer is greater than that of the lower clad layer.

23. (Amended) The nitride semiconductor device according to Claim [1] 24,
wherein said active layer has a well layer of which distance dB from the first p-
type nitride semiconductor layer is in the range of no less than 100 Å and no more than
400 Å and has a first barrier layer within the distance dB.



KOZAKI

Serial No. 09/898,461



MARKED UP ABSTRACT

In the nitride semiconductor device of the present invention, an active layer 12 is sandwiched between [a p-type] an n-type nitride semiconductor layer 11 and [an n-type] a p-type nitride semiconductor layer 13. The active layer 12 has, at least, a barrier layer 2a having an n-type impurity; a well layer 1a made of a nitride semiconductor that includes In; and a barrier layer 2c that has a p-type impurity, or that has been grown without being doped. An appropriate injection of carriers into the active layer 12 becomes possible by arranging the barrier layer 2c nearest to the p-type layer side.

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